CBCS SCHEME

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15EC71

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Microwaves and Antennas

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the general transmission line equation to find voltage and current on the line interms of position 'z' and time 't'. **(07 Marks)**

b. Describe the different mode curve in the case of reflex klystron. **(05 Marks)**

c. A transmission line has a characteristic impedance of $50 + j0.01\Omega$ and terminated in a load impedance of $73 - j42.5\Omega$ calculate : i) reflection coefficient ii) SWR. **(04 Marks)**

OR

2 a. Define relection coefficient. Derive the equation for reflection coefficient at the load end at a distance 'd' from the load. **(06 Marks)**

b. Describe the mechanism of oscillation of reflex klystron. **(06 Marks)**

c. A transmission line has the following parameters : $R = 2\Omega/m$, $G = 0.5$mmho/m, $f = 1$GHz, $L = 8$nH/m, $C = 0.23$pF/m. Calculate : i) characteristic impedance ii) propagation constant. **(04 Marks)**

Module-2

3 a. State and explain the properties of S – matrix. **(07 Marks)**

b. With a neat diagram, explain the working of precession type variable attenuator. **(06 Marks)**

c. A 20mW signal is fed into one of the collinear port 1 of a lossless H-plane T junction. Calculate the power delivered through each port when other ports are terminated in matched load. **(03 Marks)**

OR

4 a. What is magic Tee? Derive its scattering matrix. **(06 Marks)**

b. Discuss different types of coaxial connectors. **(04 Marks)**

c. 2 transmission lines of characteristic impedance Z_1 and Z_2 are joined at plane PP′. Express S–parameters in terms of impedance when each line is matched terminated. **(06 Marks)**

Module-3

5 a. Explain the construction and field pattern for microstrip line. **(06 Marks)**

b. Explain the following terms as related to antenna system :
i) directivity ii) beam efficiency iii) effective aperture. **(06 Marks)**

c. The effective apertures of transmitting and receiving antennas in a communication system are $8\lambda^2$ and $12\lambda^2$ respectively. With a separation of 1.5km between them. The EM wave travelling with frequency of 6 MHz and the total input power is 25KW. Find the power received by the receiving antenna. **(04 Marks)**

OR

6 a. Explain co-planar strip line and shielded strip line. **(06 Marks)**

b. Write a note on antenna field zones. **(06 Marks)**

c. An antenna has a field pattern given by $E(\theta) = \cos^2\theta$ for $0 \le \theta \le \pi/2$. Find the beam area and directivity. **(04 Marks)**

Module-4

7 a. Derive an expression and draw the field pattern for an array of 2 isotropic point sources with same amplitude and phase spaced $\lambda/2$ apart. **(06 Marks)**

b. Show that the radiation resistance of $\lambda/2$ antenna is 73Ω. **(06 Marks)**

c. A source has a radiation –intensity power pattern given by $U = U_m\sin^2\theta$ for $0 \le \theta \le \pi$; $0 \le \phi \le 2\pi$. Find the total power and directivity. Draw pattern. **(04 Marks)**

OR

8 a. Derive the expressions for the far field components of short dipole. **(06 Marks)**

b. Explain the principle of pattern multiplication with an example. **(06 Marks)**

c. A source has a cosine radiation intensity pattern given by $U = U_m\cos\theta$ for $0 \le \theta \le \pi/2$ and $0 \le \phi \le 2\pi$. Find the total power and directivity. **(04 Marks)**

Module-5

9 a. Derive the expression for strength $E\phi$ and $H\theta$ in case of small loop. **(06 Marks)**

b. Explain the working and design considerations of Log-periodic antenna. **(06 Marks)**

c. A 16-turn helical beam antenna has a circumference of λ and turn spacing of $\lambda/4$. Find : i) HPBW ii) axial ratio iii) directivity. **(04 Marks)**

OR

10 a. Show that the radiation resistance of small loop is $31171\left(\frac{A}{\lambda^2}\right)^2$. **(05 Marks)**

b. Write a short notes on : i) Yagi Uda array ii) parabolic reflector. **(06 Marks)**

c. Determine the length L, H-plane aperture and flare angles θ_E and θ_H of a pyramidal horn for which the E-plane aperture $a_E = 10\lambda$. Let $\delta = 0.2\lambda$ in the E-plane and 0.375λ in the H-plane. Also determine beam widths and directivity. **(05 Marks)**

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15EC72

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Image Processing

Time: 3 hrs. Max. Marks: 80

Note: *Answer FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. What is digital image? Explain the fundamental steps of digital image processing. **(08 Marks)**

b. Explain the concept of sampling and quantization of an image. **(06 Marks)**

c. Mention any four fields that use digital image processing. **(02 Marks)**

OR

2 a. Explain with neat diagram, how image is acquired using senstor strips? **(08 Marks)**

b. Define 4-, 8- and m-adjacency. Compute the lengths of the shortest 4-, 8- and m-path between p and q in the image segment shown in Fig. Q2 (b) by considering $V = \{2, 3, 4\}$ **(06 Marks)**

	3	4	1	2	0	
	0	1	0	4	2	(q)
	2	2	3	1	4	
(p)	3	0	4	2	1	
	1	2	0	3	4	

Fig. Q2 (b)

c. A common measure of transmission for digital data is the baud rate defined as the number of bits transmitted per second. Generally, transmission is accomplished in packets consisting of a start bit, a byte (8 bits) of information and a stop bit. Using these facts find how many minutes would it take to transmit a 2048×2048 image with 256 intensity levels using a 33.6 K baud modem? **(02 Marks)**

Module-2

3 a. For a given 4×4 image having gray scales between [0, 9] perform histogram equalization and draw the histogram of image before and after equalization. 4×4 image is shown in Fig. Q3 (a). **(08 Marks)**

$$\begin{bmatrix} 2 & 3 & 3 & 2 \\ 4 & 2 & 4 & 3 \\ 3 & 2 & 3 & 5 \\ 2 & 4 & 2 & 4 \end{bmatrix}$$

Fig. Q3 (a)

b. Explain smoothing of images in frequency domain using ideal, Butterworth and Gaussian Low pass filter. **(08 Marks)**

OR

4 a. Define 2D DFT- with respect to 2D DFT of an image and state the following properties:
(i) Translation (ii) Rotation (iii) Periodicity (iv) Convolution theorem. **(05 Marks)**

b. With necessary graphs, explain the log and power law transformation used for spatial image enhancement. **(05 Marks)**

c. Explain image sharpening in spatial domain using second order Laplacian derivative. **(06 Marks)**

Module-3

5 a. With necessary equations and graph, explain any four noise probability density functions. **(08 Marks)**

b. Explain minimum mean square error filtering method of restoring images. **(08 Marks)**

OR

6 a. Explain how image degradation is estimated using,
(i) Observation (ii) Mathematical modeling. **(08 Marks)**

b. Explain the order statistics filters used for restoring images in the presence of noise. **(08 Marks)**

Module-4

7 a. Write the equations for converting colors from HSI to RGB. **(06 Marks)**

b. Write H matrix for Haar transform for N = 4 and explain how it is constructed. **(04 Marks)**

c. Explain the following morphological algorithms:
(i) Thinning (ii) Thickening. **(06 Marks)**

OR

8 a. What is Pseudo color image processing? Explain intensity slicing as applied to pseudo color image processing. **(07 Marks)**

b. Explain Erosion and Dilation operations used for morphological processing. **(07 Marks)**

c. Define wavelet function. **(02 Marks)**

Module-5

9 a. Explain Marr-Hildreth edge detector. **(10 Marks)**

b. Write short note on Boundary segments. **(06 Marks)**

OR

10 a. Explain the following boundary descriptors: (i) Shape numbers (ii) Fourier descriptors. **(08 Marks)**

b. Explain Global Thresholding using Otsu's method. **(08 Marks)**

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15EC73

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Power Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Mention and explain the different types of power electronic converter systems. Draw their output/input characteristics. **(08 Marks)**

b. With neat waveforms and switching model, explain the switching characteristics of power MOSFET. **(08 Marks)**

OR

2 a. The bi-polar transistor in below figure – 2(a) is specified to have β_F in the range of 8 to 40. The load resistance is $R_c = 11\Omega$. The dc supply voltage is $V_{cc} = 200V$ and the input voltage to the base circuit is $V_B = 10V$. If $V_{CE(sat)} = 1V$ and $V_{BE(sat)} = 1.5$ V, find
i) The value of R_B that results in saturation with an ODF of 5
ii) β_{forced} iii) Power loss P_T in transistor.

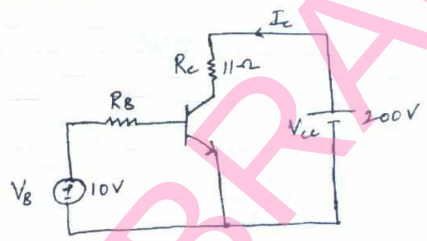

Fig Q2(a) **(08 Marks)**

b. Explain di/dt and dv/dt limitation in power converters.
A BJT is operated as a chopper switch at a frequency of $f_s = 10$ KHz. The dc voltage of the chopper is $V_s = 220$ V and the load current is $I_L = 100$A. The switching times are $t_d = 0$, $t_r = 3\mu s$ and $t_f = 1.2\ \mu s$.
Determine: i) The values of L_s, C_s and R_s for critically damped conditions.
ii) Rs, if the discharge time is limited to $1/3^{rd}$ of the switching period.
iii) Rs, if the peak discharge current is limited to 10% of the load current
iv) Power loss due to R-C snubber P_s neglecting the effect of inductor L_s on the voltage of snubber capacitor C_s. Also assume that $V_{CE(sat)} = \phi$ V **(08 Marks)**

Module-2

3 a. In detail explain the two transistor model of a thyristor. **(08 Marks)**

b. Mention and explain different thyristor turn-on methods. Mention the advantages of gate triggering. **(08 Marks)**

OR

4 a. Explain dynamic turn – off characteristics of SCR.
For R – triggering circuit, the gate voltage required to trigger the SCR is $V_{GT} = 0.6$V and corresponding $I_{GT} = 250\mu$A. The silicon diode is used and input voltage is V = 100 sin wt. Find firing angle α if $R_1 = 10k\Omega$ and $R_2 = 220k\Omega$. **(08 Marks)**

b. Explain uJT relaxation oscillator and design uJT firing circuit using an uJT having the parameters $\eta = 0.72$, $I_P = 60\mu$A, valley voltage $V_V = 2.5$ V, $I_V = 4$mA, $V_{BB} = 15$V and $R_{BB} = 5k\Omega$. The leakage current with emitter open is 3mA. The triggering frequency is 1kHz and $V_{g(min)} = 0.3$V. Also calculate the minimum and maximum values of triggering frequency. Assume C = 0.05μF. **(08 Marks)**

Module-3

5 a. With the help of neat circuit diagram describe the operation of a single phase full converter with R.L load. Draw the associated waveforms. Derive expressions for rms and average output voltages. **(08 Marks)**

b. A single phase half wave converter is operated from 120V, 60Hz supply. If the load is resistive with R = 10Ω, and the delay angle is α = 60°, calculate efficiency, FF, TUF. Also derive the equations for rms and average output voltages. **(08 Marks)**

OB

6 a. With neat circuit diagram and waveforms, explain the principle of phase angle control in AC voltage controller. Derive the equations for rms and average output voltages. **(08 Marks)**

b. A single phase half wave ac voltage controller has an input voltage of 150V and a load resistance of 8Ω. The firing angle of thyristor is 60° in each positive half cycle. Find :

i) Average output voltage ii) RMS output voltage iii) Power output

iv) Power factor (pf) v) Average input current over one cycle. **(08 Marks)**

Module-4

7 a. Classify the choppers and explain the different types and chopper circuits. **(08 Marks)**

b. Obtain an expression for the output voltage for a step-up chopper. A dc chopper has an input voltage of 200V and a load of 8Ω resistance. The voltage drop across thyristor is 2V and the chopper frequency is 800Hz. The duty cycle α = 0.4. Find

i) Average output voltage ii) rms output voltage iii) Chopper efficiency. **(08 Marks)**

OR

8 a. In detail explain buck regulator. **(08 Marks)**

b. The buck regulator shown in figure Q8 (b) has an input voltage of V_s = 12V. The required average output voltage is V_a = 5V at R = 500Ω and peak – to – peak output ripple voltage is 20mV. The switching frequency is 25kHZ. The peak – to – peak ripple current of inductor is limited to 0.8A, determine :

i) The duty cycle, K ii) The filter inductance, L iii) The filter capacitor, C

iv) The critical values of L and C.

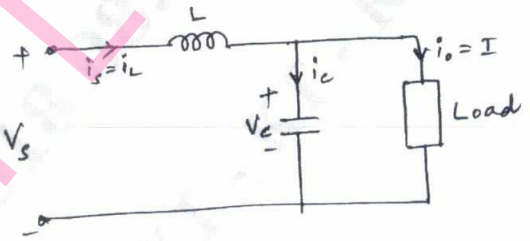

Fig Q8(b) **(08 Marks)**

Module-5

9 a. What do you mean by inverters? Explain the operation of single phase full bride inverter. Draw the load current waveforms for R, RL and RLC loads. **(08 Marks)**

b. Mention the applications of current source inverters. Explain any one type of single phase current source inverter. **(08 Marks)**

OR

10 a. Explain solid state relays. **(08 Marks)**

b. Explain microelectronic relays. **(08 Marks)**

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15EC743

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Real Time Systems

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define real time system. Classify them based on time constraints. **(06 Marks)**

b. Explain the different types of programs in system design. **(10 Marks)**

OR

2 a. Explain briefly sequence control with neat diagram. **(06 Marks)**

b. What is DDC? Explain with block diagram. **(06 Marks)**

c. Write a short note on hierarchical system. **(04 Marks)**

Module-2

3 a. What is necessity of using specialized processors in RTS? **(04 Marks)**

b. Explain the different forms of parallel computer architectures. **(12 Marks)**

OR

4 a. Explain digital input and output interface. **(08 Marks)**

b. Explain the basic interrupt input mechanism with diagram and flowchart. **(08 Marks)**

Module-3

5 a. List and explain various requirements in programming languages used in real-time applications. **(08 Marks)**

b. Explain briefly declaration and initialization of variables and constants. **(08 Marks)**

OR

6 a. What are the data types? Explain each one briefly. **(10 Marks)**

b. Write short notes on overview of real time languages. **(06 Marks)**

Module-4

7 a. Explain with neat diagram structures of RTOS. **(08 Marks)**

b. Explain cyclic and preemptive scheduling strategies. **(08 Marks)**

OR

8 a. Draw and explain task state diagram. **(08 Marks)**

b. Explain the general structures of Input Output Sub System (IOSS) **(08 Marks)**

Module-5

9 a. With neat flow-chart describe single program approach with reference to RTS design. **(08 Marks)**

b. Explain software design of RTS using software module. **(08 Marks)**

OR

10 a. Explain the outline of abstract modeling approach of ward and Mellor. **(10 Marks)**

b. Write a short note on YOURDON-METHODOLOGY. **(06 Marks)**

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15EC751

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Define LTI system. **(04 Marks)**

b. Evaluate in detail decimation and interpolation process with neat block diagram and necessary equations. **(06 Marks)**

c. Determine the interpolated sequence y(m) with input sequence x(n) = [0, 3, 6, 9] using interpolation sequence $b_k = \left[\frac{1}{3}, \frac{2}{3}, \frac{3}{3}, \frac{2}{3}, \frac{1}{3}\right]$ and interpolation factor of 3. **(06 Marks)**

OR

2 a. Define Dynamic range and resolution. **(04 Marks)**

b. Interpret the D/A converter error due to zero order hold at its output. **(06 Marks)**

c. Calculate the Dynamic range and percentage resolution of each of the following number representation formats.

i) 24-bit, single precision, fixed point format.

ii) 48-bit, double precision fixed point format

iii) A floating point format with a 16-bit mantissa and an 8-bit exponent. **(06 Marks)**

Module-2

3 a. What is Barrel shifter? **(04 Marks)**

b. Build 4×4 Barman multiplier. **(06 Marks)**

c. Analyze circular addressing mode algorithm. **(06 Marks)**

OR

4 a. Analyze MAC unit. **(04 Marks)**

b. Elaborate the importance of saturation logic and Guard bits used in MAC unit. **(06 Marks)**

c. Analyze the importance of parallelism and pipelining used in programmable DSP with the help of 8-tap FIR Filter. **(06 Marks)**

Module-3

5 a. Distinguish the architectural features of three fixed point DSPs. **(08 Marks)**

b. Sketch the functional diagram of ALU of TMS320C54XX DSP and briefly explain. **(08 Marks)**

OR

6 a. Describe the operation of Hardware timer with a neat diagram. **(08 Marks)**

b. Write an ALP of TMS320C54XX processor to compute the sum of three product terms given by an equation.

$y(n) = h_0\, x(n) + h_1\, x(n-1) + h_2\, x(n-2)$ using MAC instruction. **(08 Marks)**

Module-4

7 a. Implement the block diagram of FIR Filter and briefly explain. **(04 Marks)**
b. Sketch the block diagram for second order IIR Filter and briefly explain. **(04 Marks)**
c. Write a program to multiply two Q15 numbers. **(08 Marks)**

OR

8 a. Derive the equations to implement a butterfly structure in DITFFT algorithm. **(04 Marks)**
b. Write the subroutine for bit reversed order. **(04 Marks)**
c. Develop the subroutine to implement butterfly computation. **(08 Marks)**

Module-5

9 a. Describe DMA with respect to TMS320C54XX processor. **(08 Marks)**
b. Interface data memory system with the address range 000800H000FFFH for TMS320C5416 processor. Use 2K×8 SRAM memory chips. **(08 Marks)**

OR

10 a. With a neat block diagram, explain the synchronous serial interface between TMS320C54XX and CoDEC device. **(08 Marks)**
b. Explain the DSP based biotelemetry Receiver system with a neat block diagram. **(08 Marks)**

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